UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/045,591	10/24/2001	James R. Kohn	1376.687US1	8554

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EXAMINER
TRAN, DENISE

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 11/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>02 September 2005</u>.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 12-26* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-7* is/are allowed.

6)☒ Claim(s) *12-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some *   c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

1.   The applicant's amendment filed 9/2/05 has been considered. Claims 1-7 and

12-26 are pending in the application. Claims 8-11 have been canceled.

2.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3.   Claims 12-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Chan

et al., U.S. No. 4,513,367 (hereinafter Chan).

As per claim 23, Chan teaches a computer having a computer instruction set, the

computer instruction set comprising:

a resource-synchronization instruction that operates on a main memory location

while performing a cache-invalidate function on one or more cache lines in a local cache

(e.g., col. 3, line 60 to col. 4, line 15; col. 12, line 65 to col. 13, line 15) ;

an instruction that enables the cache-invalidate function to be performed upon

execution of the resource-synchronization instruction (e.g., col. 12, line 65 to col. 13,

line 15; col. 13, line 33-38); and

an instruction that disables the cache-invalidate function from being performed

upon execution of the resource-synchronization instruction (e.g., col. 2, lines 45-60; col.

3, lines 35-40; col. 12, line 65 to col. 13, line 15).

As per claim 21, Chan teaches an information-handling system comprising:

a memory (e.g., fig. 2, el. Main storage);

a plurality of processing elements (PEs) including a first processing element (PE)

(e.g., CP0 and CP2 or BCE0 and BCE2), wherein each one of the PEs has a cache

associated with that PE, including a first cache associated with the first PE (e.g., fig. 8,

el. 63), and wherein each one of the PEs is operatively coupled to the memory (e.g., fig.

1, connections between CP0, CP2, and main storage); and

means for enabling and disabling a cache-invalidate function from being

performed by each respective PE on its respective cache upon execution of a resource-

synchronization instruction by that respective PE (e.g., col. 12, line 65 to col. 13, line 15;

col. 13, line 33-38; and col. 2, lines 45-60; col. 3, lines 35-40; col. 12, line 65 to col. 13,

line 15), wherein the resource synchronization instruction operates on a memory

location within the memory (e.g., col. 3, line 60 to col. 4, line 15).

As per claim 12, Chan teaches an information-processing system comprising:

a first processor (e.g., fig. 1, CP0);

a first memory (e.g., fig. 1, main storage or fig. 8, cache 63 of CP2);

at least a first cache between the first processor and the first memory (e.g., fig. 8,

cache 63 of CP0) , wherein the first cache caches data accessed by the first processor

from the first memory (e.g., col. 5, lines 50-60), wherein the first processor executes:

a resource-synchronization instruction that operates on a main memory

location while performing a cache-invalidate function on one or more cache lines

in the first cache (e.g., col. 3, line 60 to col. 4, line 15; col. 12, line 65 to col. 13,

line 15);

an instruction that enables the cache-invalidate function to be performed

on one or more cache lines of the first cache upon execution of the resource-

synchronization instruction (e.g., col. 12, line 65 to col. 13, line 15; col. 13, line

33-38); and

an instruction that disables the cache-invalidate function from being

performed on one or more cache lines of the first cache upon execution of the

resource-synchronization instruction (e.g., col. 2, lines 45-60; col. 3, lines 35-40;

col. 12, line 65 to col. 13, line 15).

As per claims 13-15, 17-18, 19, 22, and 24-26, Chan teaches the use of the

resource-synchronization instruction is a test-and-set instruction (e.g. col. 3, lines 60 to

col. 4, line 12), the use of the instruction that enables the cache-invalidate function is an

enable-test-and-set-invalidate instruction or the means for enabling and disabling

includes an enable test and set instruction that enable the cache invalidate function

(e.g., col. 3, lines 60 to col. 4, line 12; col. 12, line 65 to col. 13, line 15; col. 13, line 33-

38), and the instruction that disables the cache invalidate function is a disable-test-and-

set-invalidate instruction or a disable test and set invalidate instruction that disables the

cache invalidate function (e.g., col. 3, lines 60 to col. 4, line 12; col. 2, lines 45-60; col.

3, lines 35-40; col. 12, line 65 to col. 13, line 15); the instruction that enables the cache-

invalidate function is an resource-synchronization instruction- invalidate instruction (e.g.,

col. 6, lines 30-35; col. 3, lines 60 to col. 4, line 12; col. 12, line 65 to col. 13, line 15;

col. 13, lines 33-38), and the instruction that disables the cache invalidate function is a

disable- resource-synchronization instruction -invalidate instruction (e.g., col. 6, lines

30-35; col. 3, lines 60 to col. 4, line 12; col. 2, lines 45-60; col. 3, lines 35-40; col. 12,

line 65 to col. 13, line 15).

As per claims 16 and 20, Chan teaches a second processor (e.g., fig. 1, cp2),

and at least a second cache between the second processor and the first memory (e.g.,

fig. 8, cache 63 of cp2), wherein the second cache caches data accessed by the second

processor from the first memory (e.g., col. 5, lines 50-60), wherein the second

processor executes: the resource-synchronization instruction (e.g., col. 3, line 60 to col.

4, line 15; col. 12, line 65 to col. 13, line 15); the instruction that enables a cache-

invalidate function to be performed upon execution of the resource-synchronization

instruction (e.g., col. 12, line 65 to col. 13, line 15; col. 13, line 33-38); and the

instruction that disables the cache-invalidate function from being performed upon

execution of the resource-synchronization instruction(e.g., col. 2, lines 45-60; col. 3,

lines 35-40; col. 12, line 65 to col. 13, line 15); Chan teaches wherein the cache-

invalidate function invalidates the entire first cache (e.g., col. 7, lines 45-50 when all

valid bits are not valid).

4.   Claims 1-7 are allowable over the prior of record.

5. Applicant's arguments filed 9/2/05 have been fully considered but they are not persuasive.

6. In the remarks, the applicant argued that there is no teaching in Chan of an instruction enables the cache invalidate function to be perform on one or more cache lines of the first cache upon execution of the resource-synchronization instruction.

The examiner disagreed with the applicant's argument. As stated in the previous Office Action, paragraph 5, Chan teaches a resource-synchronization instruction that operates on a main memory location while performing a cache-invalidate function on one or more cache lines in a local cache (e.g., col. 3, line 60 to col. 4, line 15; col. 12, line 65 to col. 13, line 15) ; and an instruction that enables the cache-invalidate function to be performed upon execution of the resource-synchronization instruction (e.g., col. 12, line 65 to col. 13, line 15; col. 13, line 33-38). For example, col. 12, line 65 to col. 13, line 15, Chan teaches "A cache miss command (show in FIG. 4) occurs if any CP(I) request . . . when the CP(I) issues a store-interrogate (SI) request which require that CD(I) cross interrogate each CD . . . invalidates any remote copy of the requested line;" col. 3, line 60 to col. 4, line 15 "locking control . . . test and set . . . ." Therefore, Chan teaches a cache invalidate instruction upon resource synchronization.

Also, in response to applicant's argument, Chan, teaches an instruction enable a cache invalidate function upon execution of a resource synchronization instruction (e.g., col. 8, lines 30-40 and col. 45-50). That is an instruction can unlock the bits upon

an execution of synchronization instruction (e.g., col. 3, line 60 to col. 4, line 15; col. 6,

lines 30-45).

7.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the mailing date of this final action.

8.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Denise Tran whose telephone number is (571) 272-

4189. The examiner can normally be reached on Monday, Thursday, and Friday from

8:45a.m. to 5:15p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Matt Kim, can be reached on (571) 272-4182. The fax phone number for

the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DT

11/8/05